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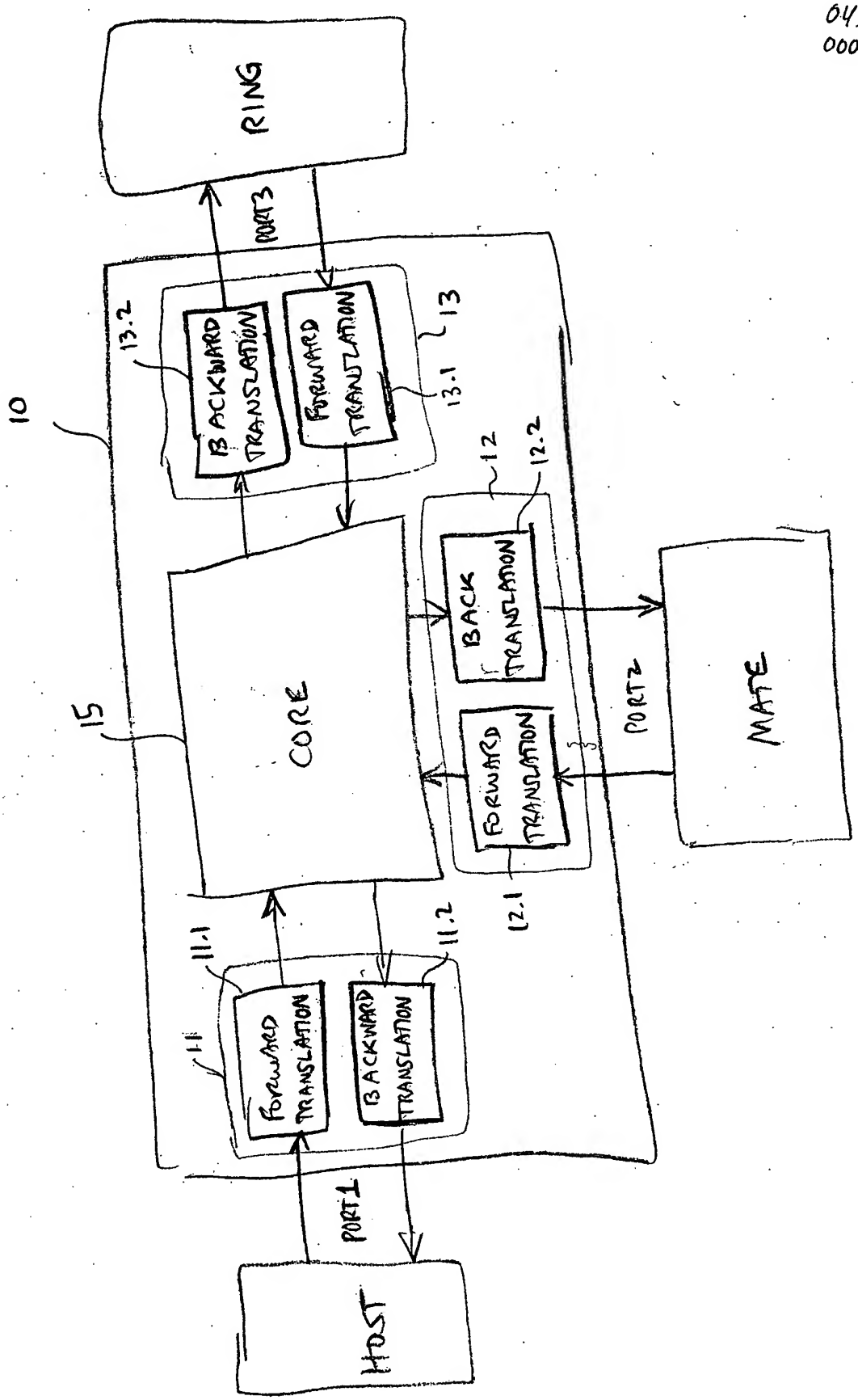

FIG. 1

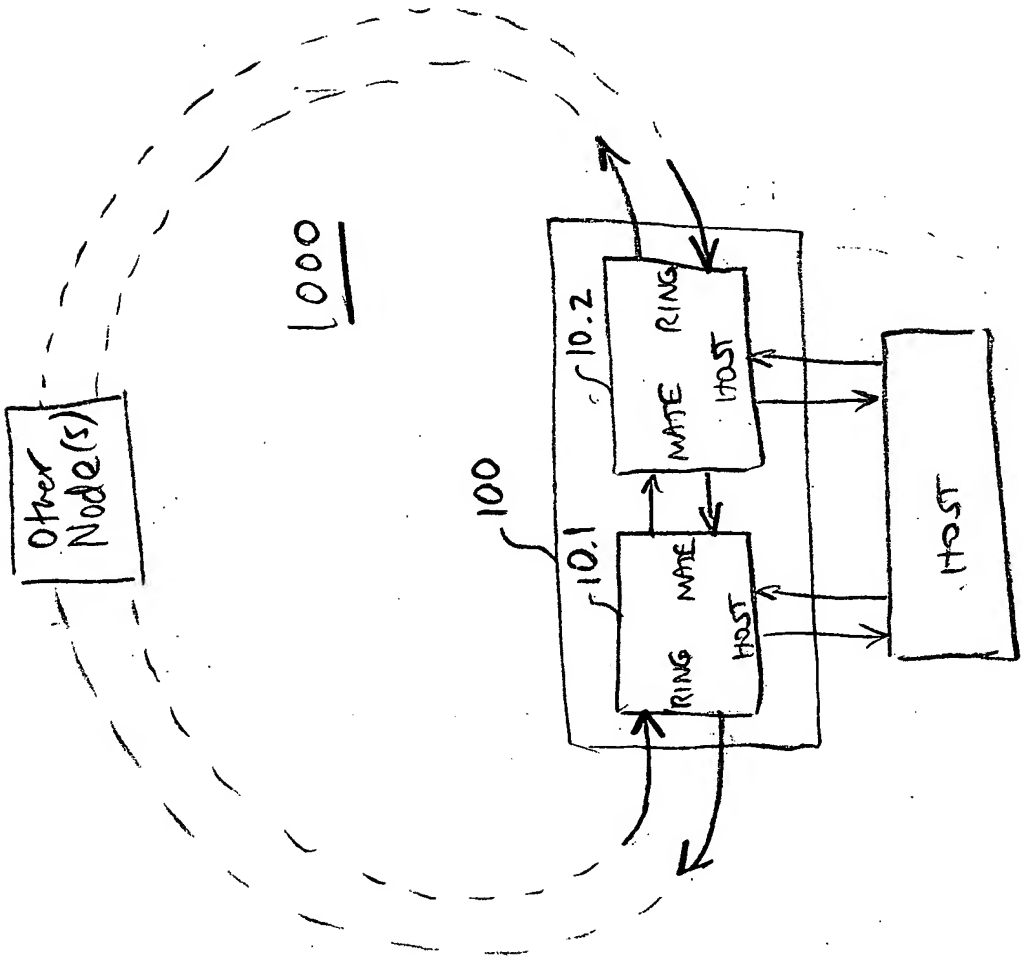

FIG. 1A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME TO LIVE								RI	MODE			PRIORITY			P

FIG. 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME TO LIVE								RI	MODE		FE	PRTY.		WE	P

FIG. 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME TO LIVE								RI	MODE		FE	PRTY.		WE	P

FORWARD MAPPING

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME TO LIVE								RI	MODE		1	PRTY.		WE	FE

FIG. 4

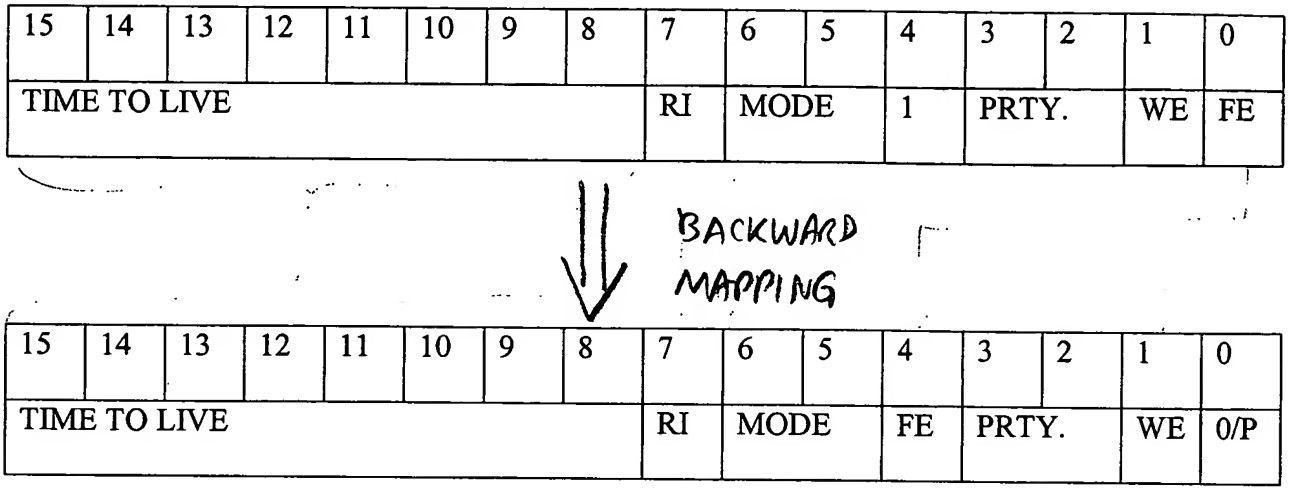
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
TIME TO LIVE
RI
MODE
1
PRTY.
WE
FE
BACKWARD MAPPING
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
TIME TO LIVE
RI
MODE
FE
PRTY.
WE
0/P

FIG. 5

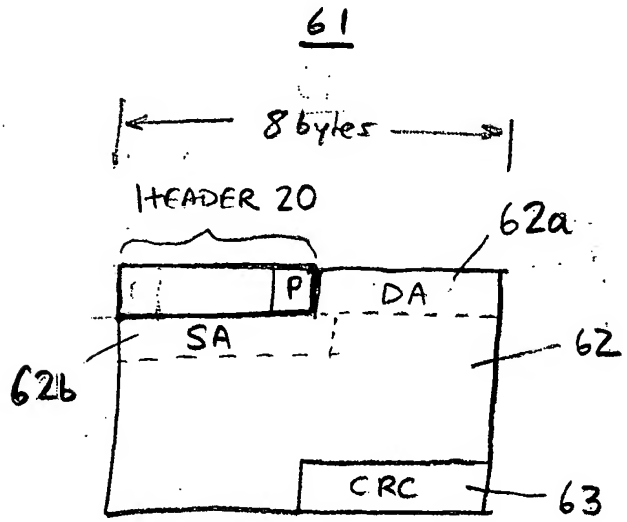
61
8 bytes
HEADER 20
62a
P
DA
SA
62b
62
CRC
63

FIG. 6A

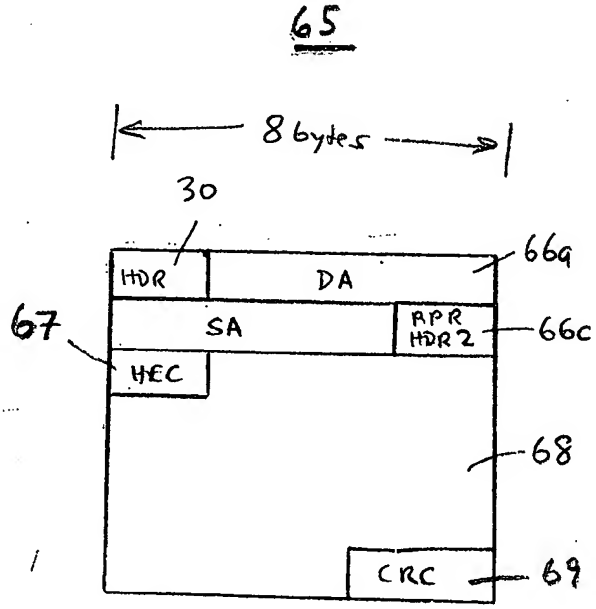
65
8 bytes
30
HDR
DA
66a
67
SA
RPR HDR 2
66c
HEC
68
CRC
69

FIG. 6B

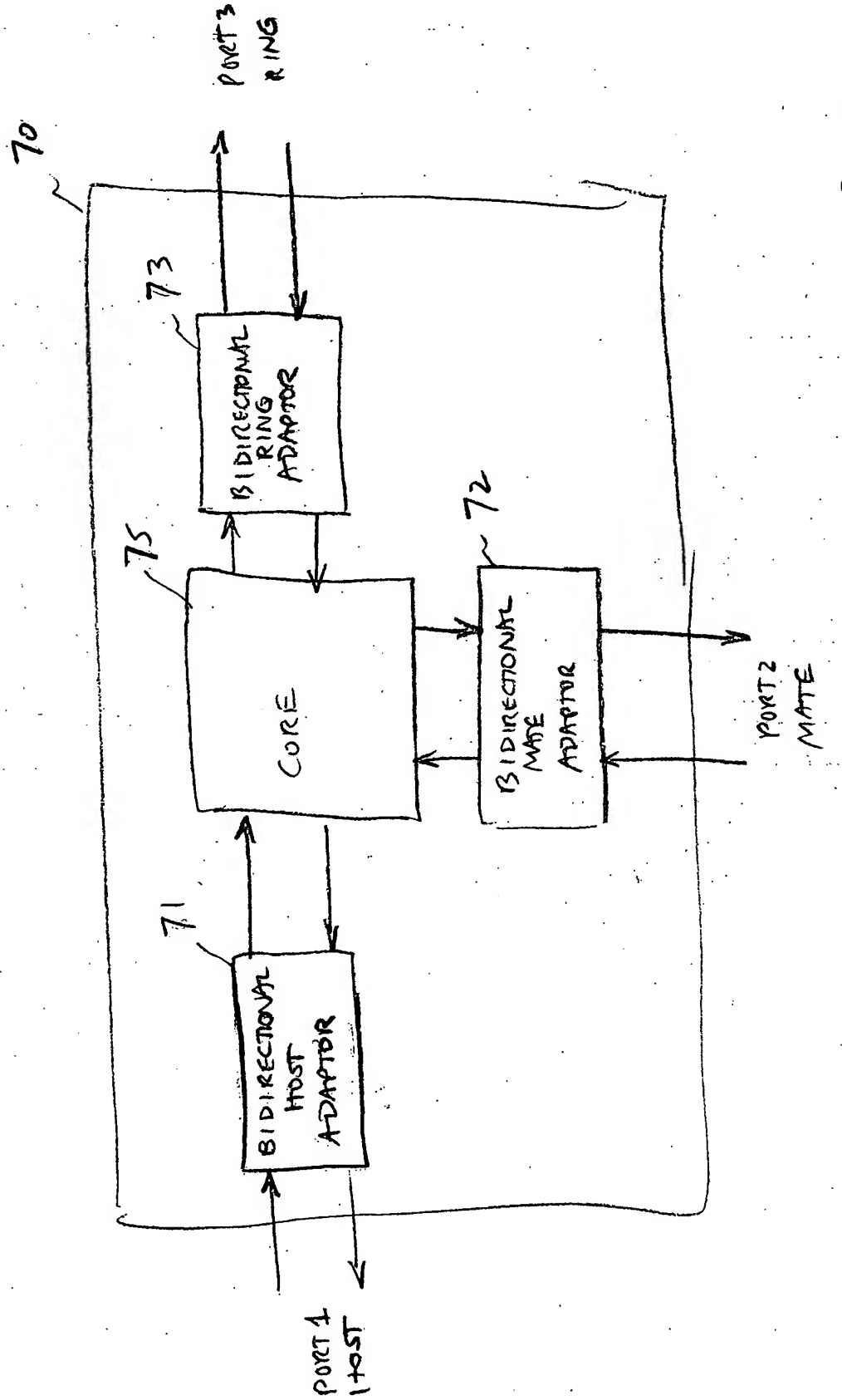
70
PORT 3
RING
73
BIDIRECTIONAL
RING
ADAPTOR
75
CORE
72
BIDIRECTIONAL
MATE
ADAPTOR
PORT 2
MATE
71
BIDIRECTIONAL
HOST
ADAPTOR
PORT 1
HOST

FIG. 7

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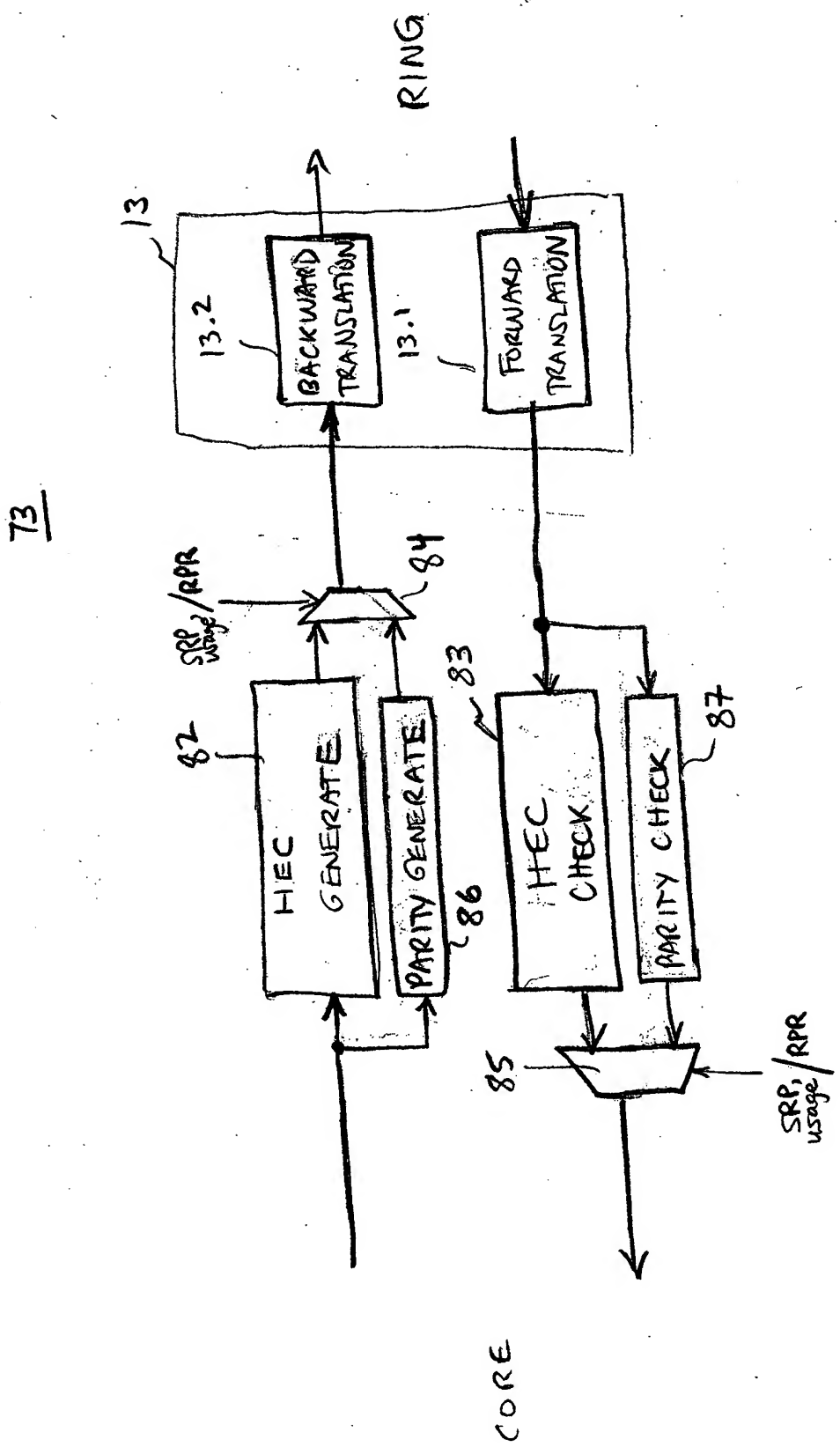

FIG. 8

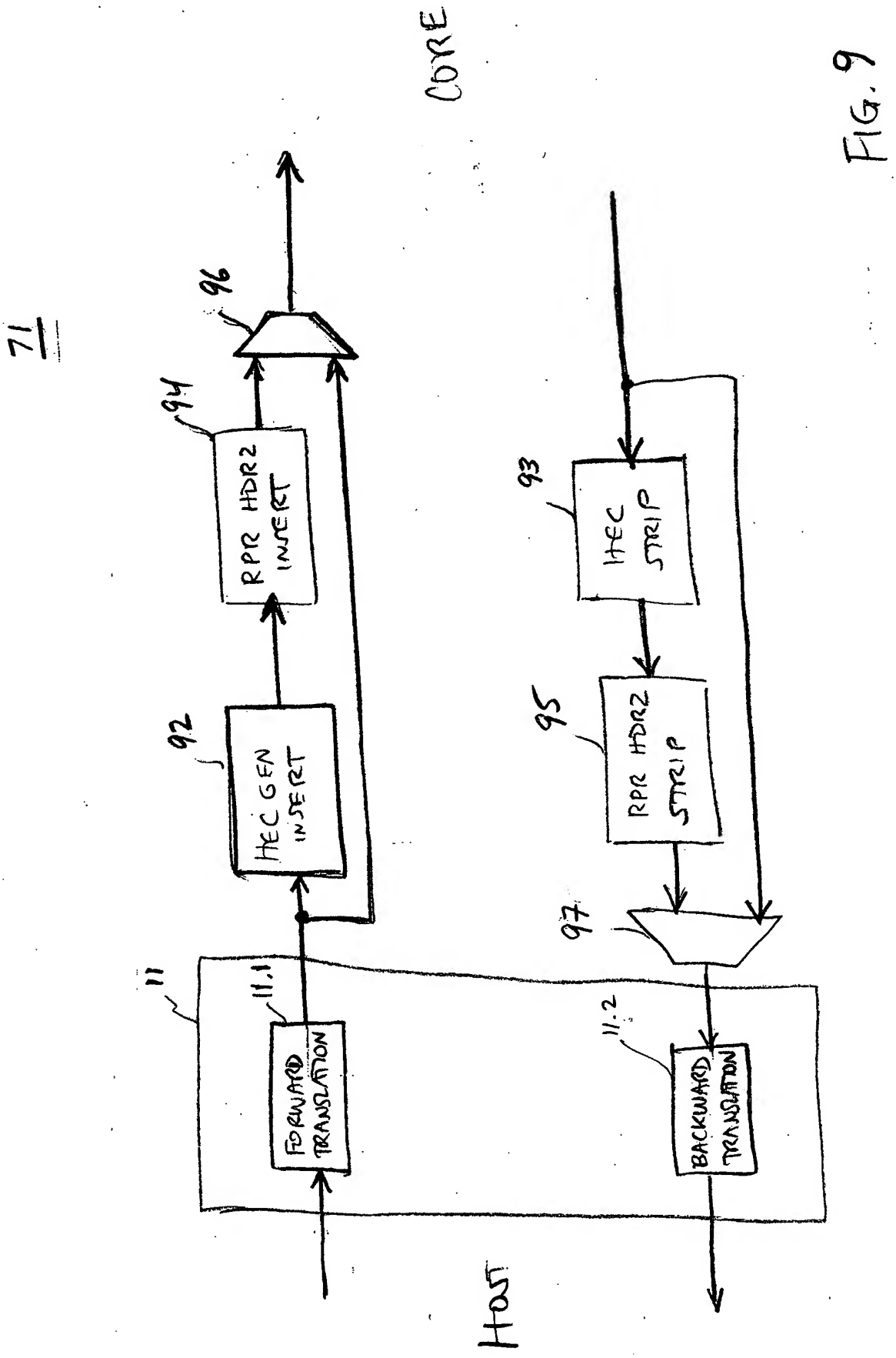
71
CORE
96
94
RPR HDR2 INSERT
92
HEC GEN INSERT
93
HEC STRIP
95
RPR HDR2 STRIP
97
11
11.1
FORWARD TRANSLATION
11.2
BACKWARD TRANSLATION
HOST

FIG. 9